AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

Claim 1 (currently amended): A microcomputer having an at least partially erasable built-in nonvolatile memory including:

a communication circuit for receiving a test program for said nonvolatile memory from an external check system;

a RAM on which said test program is run; and

a boot ROM comprising a control program for, upon receiving a test command issued by the external check system, enabling said receiving of said test program from said external check system using said communication circuit and running of said test program on said RAM,

wherein said boot ROM is detached from said nonvolatile memory.

Claim 2 (canceled)

Claim 3 (currently amended): A microcomputer having an at least partially erasable built-in nonvolatile memory including:

a nonvolatile memory;

a boot ROM, wherein said boot ROM is detached from said nonvolatile memory;

a RAM;

a CPU for running a program stored in said boot ROM and RAM; and

a communication circuit for controlling a communication with a check system,

said boot ROM having stored a control program for jobs of:

upon receiving a test command issued from said check system, receiving a test program for said nonvolatile memory from said check system to be stored in said RAM;

running said test program; and

sending a test result to said check system.

Claim 4 (currently amended): A check system of an at least partially erasable built-in nonvolatile memory in a microcomputer furnished with:

at least one external communication device connected to said microcomputer in such a manner so as to allow a communication in a one-to-one correspondence,

each external communication device including,

a storage device having stored a test program for said built-in nonvolatile memory in said microcomputer, and

a communication microcomputer for sending said test program to said microcomputer,

wherein said microcomputer includes a boot ROM comprising a control program for, upon receiving a test command issued by the corresponding external communication device, enabling receiving of said test program from said corresponding external communication device using a communication circuit and running of the test program on a RAM, and

wherein said boot ROM is detached from said nonvolatile memory.

Claim 5 (original): The check system of Claim 4, further furnished with a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively.

Claim 6 (currently amended): A check system of an at least partially erasable built-in nonvolatile memory in a microcomputer furnished with an external communication device including:

a storage device having stored a test program for said microcomputer having said built-in nonvolatile memory;

a communication control circuit for controlling a communication with said microcomputer; and

a communication microcomputer for sending said test program to said microcomputer when checking the built-in nonvolatile memory therein,

wherein said microcomputer includes a boot ROM comprising a control program for, upon receiving a test command issued by the external communication device, enabling receiving of said test program from said external communication device using a communication circuit and running of the test program on a RAM, and

wherein said boot ROM is detached from said nonvolatile memory.

Claim 7 (original): The check system of Claim 6, further furnished with a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively.

Claim 8 (currently amended): An IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory including:

a communication circuit for receiving a test program for a nonvolatile memory from an external check system;

a RAM on which said test program is run, and

a boot ROM comprising a control program for, upon receiving a test command issued by the external check system, enabling said receiving of said test program from said external check system using said communication circuit and running of said test program on said RAM,

wherein said boot ROM is detached from said nonvolatile memory.

Claim 9 (canceled)

Claim 10 (currently amended): An IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory including:

said at least partially erasable nonvolatile memory;

a boot ROM, wherein said boot ROM is detached from said nonvolatile memory;

a RAM;

a CPU for running a program stored in said boot ROM and RAM; and

a communication circuit for controlling a communication with a check system,

said boot ROM having stored a control program for jobs of:

upon receiving a test command issued from said check system, receiving a test program for said nonvolatile memory from said check system to be stored in said RAM;

running said test program; and

sending a test result to said check system.

Claim 11 (currently amended): A check system of an IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory furnished with:

at least one external communication device connected to said microcomputer packed in said IC card in such a manner so as to allow a communication in a one-to-one correspondence,

each external communication device including,

a storage device having stored a test program for said built-in nonvolatile memory in said microcomputer, and

a communication microcomputer for sending said test program to said IC card,

wherein said microcomputer includes a boot ROM comprising a control program for, upon receiving a test command issued by the corresponding external communication device, enabling receiving of said test program from said

corresponding external communication device using a communication circuit and running of the test program on a RAM, and

wherein said boot ROM is detached from said nonvolatile memory.

Claim 12 (original) The check system of Claim 11, further furnished with a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively.

Claim 13 (currently amended) A check system of an IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory furnished with an external communication device including:

a storage device having stored a test program for said built-in nonvolatile memory in said microcomputer packed in said IC card;

a communication control circuit for controlling a communication with said IC card; and

a communication microcomputer for sending said test program to said IC card when checking said built-in nonvolatile memory,

wherein said microcomputer includes a boot ROM comprising a control program for, upon receiving a test command issued by the external communication device, enabling receiving of said test program from said external communication device using a communication circuit and running of the test program on a RAM, and

wherein said boot ROM is detached from said nonvolatile memory.

Claim 14 (original) The check system of Claim 13, further furnished with a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively.

Claim 15 (previously presented) The microcomputer of Claim 1, further comprising a plurality of microcomputers each having a built-in nonvolatile memory, and wherein said check system comprises a control computer connected to a plurality of external communication devices, for intensively controlling a check-up of said plurality of microcomputers each connected to said plurality of external communication devices, respectively, and

each of said plurality of microcomputers including a boot ROM comprising a control program for, upon receiving a test command issued by the control computer, enabling receiving of said test program from said control computer through a communication circuit and running of said test program on said RAM.

Claim 16 (previously presented) The microcomputer of Claim 3, further comprising a plurality of microcomputers having a built-in nonvolatile memory, and wherein said check system comprises a control computer connected to a plurality of external communication devices, for intensively controlling a check-up of said plurality of said microcomputers each connected to said plurality of external communication devices, respectively, and

each of said plurality of microcomputers including a boot ROM having stored a control program for jobs including upon receiving a test command issued

from said control computer, receiving said test program for said nonvolatile memory from said check system to be stored in said RAM.

Claim 17 (previously presented) The check system of claim 5, wherein each of said plurality of microcomputers including a boot ROM comprising a control program for, upon receiving a test command issued by said control computer, enabling receiving of said test program from said control computer through a communication circuit and running of said test program on said RAM.

Claim 18 (previously presented) The check system of claim 7, wherein each of said plurality of microcomputers including a boot ROM comprising a control program for, upon receiving a test command issued by said control computer, enabling receiving of said test program from said control computer through a communication circuit and running of said test program on said RAM.

Claim 19 (previously presented) The microcomputer of claim 1, wherein enabling said receiving of said test program performed by the control program of said boot ROM comprises allocating an area on said RAM sufficient to receive the test program and controlling said communication circuit to receive and transmit the test program to said RAM.

Claim 20 (previously presented) The microcomputer of claim 3, wherein said receiving of said test program performed by the control program stored in said boot ROM comprises allocating an area on said RAM sufficient to receive

the test program and controlling said communication circuit to receive and transmit the test program to said RAM.

Claim 21 (previously presented) The check system of claim 4, wherein enabling said receiving of said test program performed by the control program of said boot ROM comprises allocating an area on said RAM sufficient to receive the test program and controlling said communication circuit to receive and transmit the test program to said RAM.

Claim 22 (previously presented) The check system of claim 6, wherein enabling said receiving of said test program performed by the control program of said boot ROM comprises allocating an area on said RAM sufficient to receive the test program and controlling said communication circuit to receive and transmit the test program to said RAM.

Claim 23 (canceled).

Claim 24 (canceled).